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April 19, 2004

MAIL STOP DD
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: App No. 10/804,452; "Memory Expansion and Integrated Circuit Stacking
System and Method"
Docket No. 0254-094-PCT-2-C1

Dear Commissioner:

Please find enclosed for filing the following:

1. Information Disclosure Statement;
2. Form 1449 (and one duplicate copy);
3. 102 references; and
4. a return postcard for confirmation of receipt.

The Commissioner is hereby authorized to charge any fees which may be required to Deposit Account 50-0897. Please return the postcard confirming your receipt of the enclosed materials.

Yours truly,

ANDREWS & KURTH LLP

Pam Menke
Board Certified Legal Assistant in Civil Trial Law
Texas Board of Legal Specialization

/pm
enclosures



Attorney Docket No.: 0254-094-PCT-2-C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: Memory Expansion and Integrated Circuit Stacking System and Method

Application No.: 10/804,452

Filing Date: 03/19/2004

Inventor: Russell Rapport, et al.

Assignee: Staktek Group, L.P.

Examiner: ~~TBA~~ A.A.

Group: ~~TBA~~ 2841

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Pursuant to the guidelines for Information Disclosure Statements, 37 C.F.R. §§ 1.97-1.98, attached hereto is PTO Form 1449 (six sheets) with references listed for consideration by the Office.

In accordance with 37 C.F.R. § 1.98(a), copies of the listed written references are being provided.

In accordance with 37 C.F.R. §§ 1.97(g)-(h), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b) or prior art under 35 U.S.C. §§ 102 or 103.

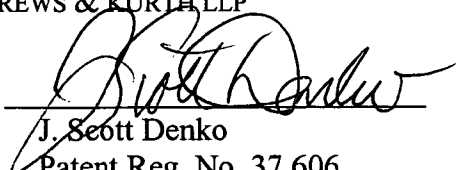


This Information Disclosure Statement is being filed before receipt of the first Office action, so no fee is believed to be due. The Commissioner is hereby authorized to charge any fees which may be required in connection with the filing, or to credit any overpayment to Deposit Account No. 50-0897, upon which account the undersigned has the authority to sign. A duplicate copy of Form 1449 is enclosed.

Respectfully submitted,

ANDREWS & KURTH LLP

April 19, 2004
Date

By: 
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Form PTO-1449 (Modified)
(Rev. 11/92)U.S. Dept. of Commerce
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ATTY. DOCKET NO.

SERIAL NO.

0254-094-PCT-2-C1

10/804,452

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

APPLICANT

Rapport, et al

FILING DATE

3/19/04

GROUP

2841

(37 CFR 1.98(b))

U.S. PATENT DOCUMENTS

*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
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/A.A./	5,159,434	10/27/1992	Kohno, et al	357/80		02/01/1991
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/A.A./	5,313,097	05/17/1994	Haj-Ali-Ahmadi, et al	257/706		11/16/1992
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/A.A./	5,484,959	01/16/1996	Burns	174/524		12/11/1992
/A.A./	5,572,065	11/05/1996	Burns	257/666		10/24/1994
/A.A./	5,612,570	03/18/1997	Eide, et al	257/686		04/13/1995
/A.A./	5,644,161	07/01/1997	Burns	257/668		06/07/1995
/A.A./	5,776,797	07/07/1998	Nicewarner, Jr., et al	438/107		07/02/1997
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FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

Document Number	Date	Country	Class	Subclass	Translation	
					Yes	No

OTHER DOCUMENTS

(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

EXAMINER	/Andargie Aychillhum/	DATE CONSIDERED	07/02/2007
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*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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(37 CFR 1.98(b))

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*Examiner *Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
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/A.A./	5,805,422	09/08/1998	Otake, et al	361/749		08/15/1997
/A.A./	5,869,353	02/09/1999	Levy, et al	438/109		11/17/1997
/A.A./	5,926,369	07/20/1999	Ingraham, et al	361/699		01/22/1998
/A.A./	5,949,657	09/07/1999	Karabatsos	361/803		08/25/1998
/A.A./	6,014,316	01/11/2000	Eide	361/735		6/10/1998
/A.A./	6,172,874B1	01/09/2001	Bartilson	361/719		04/06/1998
/A.A./	6,208,521B1	3/27/2001	Nakatsuka	361/749		5/19/1998
/A.A./	6,225,688B1	05/01/2001	Kim et al.	257/686		02/04/1999
/A.A./	6,281,577B1	08/28/2001	Oppermann et al.	257/724		04/22/1997
/A.A./	6,392,162B1	05/21/2002	Karabatsos	174/261		11/10/2000

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/A.A./	6,097,087	8/1/2000	Farnworth, Warren M. et al	257/698		10/31/1997
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/A.A./	6,368,896B2	4/9/2002	Farnworth, Warren M. et al	438/113		4/23/1999
/A.A./	6,410,857B1	6/25/2002	Gonya	174/254		8/13/2001
/A.A./	6,426,240B2	7/30/2002	Isaak	438/106		6/25/2001
/A.A./	6,426,549B1	7/30/2002	Isaak, Harlan R.	257/686		11/3/2000
/A.A./	6,444,921B1	9/3/2002	Wang, et al	174/260		2/3/2000
/A.A./	6,465,877B1	10/15/2002	Farnworth, Warren M. et al	257/668		3/27/2000
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						Yes	No
/A.A./	58-96756(A)	06/08/1983	Japan			Partial	
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		Dense-Pac Microsystems, Breaking Space Barriers, 3-D Technology 1993
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		"Design Techniques for Ball Grid Arrays," William R. Newberry, Xynetix Design Systems, Inc.

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/A.A./	6,208,521B1	3/27/2001	Nakatsuka, Yasuo	361/749		5/19/1998
/A.A./	6,265,660B1	7/24/2001	Tandy, Patrick W.	174/52.4		8/18/2000
/A.A./	6,300,679B1	10/9/2001	Mukerji et al.	257/738		6/1/1998
/A.A./	6,462,412B2	10/8/2002	Kamei et al	257/723		1/17/2001
/A.A./	6,465,893B1	10/15/2002	Khandros et al.	257/777		10/19/2000
/A.A./	6,486,544B1	11/26/2002	Hashimoto, Nobuaki	257/686		9/3/1999
/A.A./	6,560,117B2	5/6/2003	Moon, Ow Chee	361/749		8/30/2001
/A.A./	6,590,282B1	7/8/2003	Wang et al.	257/686		4/12/2002
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	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
/A.A./	62-230027(A)	10/08/1987	Japan			Partial	

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/	"Chip Scale Packaging and Redistribution," Paul A. Magill, Glenn A. Rinne, J. Daniel Mis, Wayne C. Machon, Joseph W. Baggs, Unitive Electronics Inc.
/	"3D Interconnection for Ultra-Dense Multichip Modules," Christian VAL, Thomson-CSF DCS Computer Division, Thierry Lemoine, Thomson-CSF RCM Radar Countermeasures Division
/	"High Density Memory Packaging Technology High Speed Imaging Applications," Dean Frew, Texas Instruments Incorporated
/	Teresa Technologies, Inc. – Semiconductor Intellectual Property, Chip Scale Packaging – Website pages (3)

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/A.A./	US2002/0006032A1	01/17/2002	Karabatsos	361/760		01/11/2001
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/A.A./	4,891,789	01/02/1990	Quattrini, et al	365/63		03/03/1988
/A.A./	5,261,068	11/09/1993	Gaskins, et al.	395/425		05/25/1990
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Document Number	Date	Country	Class	Subclass	Translation	
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OTHER DOCUMENTS

(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

/A.A./	/Tessera Introduces uZ™ - Ball Stacked Memory Package for Computing and Portable Electronic Products" Joyce Smaragdis, Tessera Public Relations; 2 figures that purport to be directed to the uZ™ - Ball Stacked Memory Package.
/A.A./	/Ron Bauer, Intel. "Stacked-CSP Delivers Flexibility, Reliability, and Space-Saving Capabilities", Spring 2002.
/A.A./	Tessera uZ Ball Stack Package. 4 figures that purport to be directed to the uZ - Ball Stacked Memory, 1 Page.
/A.A./	"Vertically-Intergrated Package," Alvin Weinberg, Pacesetter, Inc. and W. Kinzy Jones, Florida International University

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/A.A./	6,620,651B2	9/16/2003	He et al.	438/113		10/23/2001
/A.A./	US2002/0139577A1	10/3/2002	Miller, Charles A.	174/261		3/27/2001
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/A.A./	3,436,604	04/01/1969	Hyltin	317/101		04/25/1966
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/A.A./	4,288,841	09/08/1981	Gogal	361/414		09/20/1979
/A.A./	4,696,525	09/29/1987	Coller, et al	439/69		12/13/1985
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/A.A./	4,911,643	03/27/1990	Perry, et al	439/67		08/03/1989
/A.A./	4,953,060	08/28/1990	Lauffer, et al	361/388		05/05/1989
/A.A./	4,956,694	09/11/1990	Eide	357/74		11/04/1988
/A.A./	4,983,533	01/08/1991	Go	437/7		10/28/1987

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						Yes	No

OTHER DOCUMENTS

(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

/A.A./	3	Dense-Pac Microsystems, 256 Megabyte CMOS DRAM DP3ED32MS72RW5
/A.A./	✓	IBM Preliminary 168 Pin SDRAM Registered DIMM Functional Description & Timing Diagrams

EXAMINER /Andargie Aychillhum/

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